

## I N T H E S P E C I F I C A T I O N

**Please amend the paragraph beginning at page 7, line 5 to read as follows:**

In the absence of the third current ~~source~~ mirror 338, the discharging portion 206 would fail to provide a sharp shut-off, thereby compromising high speed performance. However, with the third current source, the common drain node 316 is promptly pulled up to the supply voltage, so that the first and second current mirrors accurately follow the turning off of the transistor 304.

## I N T H E C L A I M S

1. (Original) A charge pump comprising:

a first PMOS transistor;

a first NMOS transistor coupled to the first PMOS transistor via a first common drain node;

a second PMOS transistor;

a second NMOS transistor coupled to the second PMOS transistor via a second common drain node;

a first current source coupled to respective source terminals of the first and second PMOS transistors;

a second current source coupled to respective source terminals of the first and second NMOS transistors;

a first operational amplifier having a first input coupled to the first common drain node and a second input coupled to the second common drain node;

a reference circuit; and

a second operational amplifier having a first input coupled to the first common drain node and a second input coupled to the reference circuit.

2. (Original) The charge pump of claim 1, further comprising a capacitor coupled to the first common drain node.

3. (Original) The charge pump of claim 1, wherein the reference circuit includes:

a third PMOS transistor;

a third NMOS transistor coupled to the third PMOS transistor via a third common drain node;

a third current source coupled to a source terminal of the third PMOS transistor; and  
a fourth current source coupled to a source terminal of the third NMOS transistor;  
wherein the second input of the second operational amplifier is coupled to the third common drain node.

4. (Original) The charge pump of claim 1, wherein the first current source is a PMOS current source.

5. (Original) The charge pump of claim 1, wherein the second current source is an NMOS current source.

6. (Original) The charge pump of claim 1, wherein an output of the first operational amplifier is coupled to the second common drain node.

7. (Original) The charge pump of claim 1, wherein an output of the second operational amplifier is coupled to a gate terminal of the first current source.

8. (Original) An apparatus comprising:

a communication port; and

a serializer/deserializer coupled to the communication port, the serializer/deserializer including a phase locked loop, the phase locked loop including a charge pump, the charge pump including:

a first PMOS transistor;

a first NMOS transistor coupled to the first PMOS transistor via a first common drain node;

a second PMOS transistor;

a second NMOS transistor coupled to the second PMOS transistor via a second common drain node;

a first current source coupled to respective source terminals of the first and second PMOS transistors;

a second current source coupled to respective source terminals of the first and second NMOS transistors;

a first operational amplifier having a first input coupled to the first common drain node and having a second input and an output both coupled to the second common drain node;

a reference circuit; and

a second operational amplifier having a first input coupled to the first common drain node, a second input coupled to the reference circuit, and an output coupled to a gate terminal of the first current source.

9. (Original) The apparatus of claim 8, wherein the charge pump further includes a capacitor coupled to the first common drain node.

10. (Original) The apparatus of claim 8, wherein the reference circuit includes:

a third PMOS transistor;

a third NMOS transistor coupled to the third PMOS transistor via a third common drain node;

a third current source coupled to a source terminal of the third PMOS transistor; and

a fourth current source coupled to a source terminal of the third NMOS transistor;

wherein the second input of the second operational amplifier is coupled to the third common drain node.

11. (Original) The apparatus of claim 8, wherein the first current source is a PMOS current source.

12. (Original) The apparatus of claim 8, wherein the second current source is an NMOS current source.

13. (Original) The apparatus of claim 8, wherein an output of the first operational amplifier is coupled to the second common drain node.

14. (Original) The apparatus of claim 8, wherein an output of the second operational amplifier is coupled to a gate terminal of the first current source.

15. (Original) A charge pump comprising:

- an input differential pair including a first transistor and a second transistor;

- a first current mirror coupled to a drain terminal of the second transistor via a common drain node;

- a second current mirror coupled to the first current mirror and coupled to an output terminal of the charge pump to selectively discharge the output terminal; and

- a third current mirror coupled as a load to the first transistor and coupled to the common drain node to selectively pull up the common drain node.

16. (Original) The charge pump of claim 15, wherein the first current mirror is formed of PMOS devices.

17. (Original) The charge pump of claim 15, wherein the second current mirror is formed of NMOS devices.

18. (Original) The charge pump of claim 15, wherein the third current mirror is formed of PMOS devices.

19. (Original) The charge pump of claim 15, further comprising a capacitor coupled to the output terminal.

20. (Original) An apparatus comprising:

a communication port; and

a serializer/deserializer coupled to the communication port, the serializer/deserializer including a phase locked loop, the phase locked loop including a charge pump, the charge pump including:

an input differential pair including a first transistor and a second transistor;

a first current mirror coupled to a drain terminal of the second transistor via a common drain node;

a second current mirror coupled to the first current mirror and coupled to an output terminal of the charge pump to selectively discharge the output terminal; and

a third current mirror coupled as a load to the first transistor and coupled to the common drain node to selectively pull up the common drain node.

21. (Original) The apparatus of claim 20, wherein the first current mirror is formed of PMOS devices.

22. (Original) The apparatus of claim 20, wherein the second current mirror is formed of NMOS devices.

23. (Original) The apparatus of claim 20, wherein the third current mirror is formed of PMOS devices.

24. (Original) The apparatus of claim 20, further comprising a capacitor coupled to the output terminal.

25. (New) A charge pump comprising:

- an output terminal;

- a first element to control charging of the output terminal;

- a second element to control discharging of the output terminal and including a common node with the first element;

- a reference circuit; and

- an operational amplifier including a first input coupled to the common node and a second input coupled to the reference circuit.

26. (New) The charge pump of claim 25, wherein the first element comprises a first transistive element and the second element comprises a second transistive element.

27. (New) The charge pump of claim 26, wherein the first element comprises a PMOS transistor and the second element comprises an NMOS transistor.

28. (New) The charge pump of claim 25, wherein the reference circuit includes:

- a first transistive element;

- a second transistive element coupled to the first transistive element;

- a first current source coupled to the first transistive element; and

- a second current source coupled to the second transistive element.

29. (New) The charge pump of claim 28, wherein the first transistive element comprises a PMOS transistor and the second transistive element comprises an NMOS transistor.

30. (New) The charge pump of claim 29, wherein:

- the first and second transistive elements include a common drain node; and

- the second input of the operational amplifier is coupled to the common drain node.

31. (New) The charge pump of claim 25, further comprising:

- a second output terminal; and

- a second operational amplifier including a first input coupled to the common node and including a second input coupled to the second output terminal.

32. (New) An apparatus comprising:

- a communication port; and

- a serializer/deserializer coupled to the communication port, the serializer/deserializer including a phase locked loop, the phase locked loop including a charge pump, the charge pump including:

  - an output terminal;

  - a first element to control charging of the output terminal;

  - a second element to control discharging of the output terminal and including a common node with the first element;

  - a reference circuit; and

  - an operational amplifier having a first input coupled to the common node and a second input coupled to the reference circuit.

33. (New) The apparatus of claim 32, wherein the first element comprises a first transistive element and the second element comprises a second transistive element.

34. (New) The apparatus of claim 33, wherein the first element comprises a PMOS transistor and the second element comprises an NMOS transistor.

35. (New) The apparatus of claim 32, wherein the reference circuit includes:

- a first transistive element;

- a second transistive element coupled to the first transistive element;

- a first current source coupled to the first transistive element; and

- a second current source coupled to the second transistive element.

36. (New) The apparatus of claim 35, wherein the first transistive element comprises a PMOS transistor and the second transistive element comprises an NMOS transistor.

37. (New) The apparatus of claim 36, wherein:

- the first and second transistive elements include a common drain node; and
- the second input of the operational amplifier is coupled to the common drain node.

38. (New) The apparatus of claim 32, wherein the charge pump further includes:

- a second output terminal; and

- a second operational amplifier include a first input coupled to the common node and include a second input coupled to the second output terminal.

## **D R A W I N G   A M E N D M E N T**

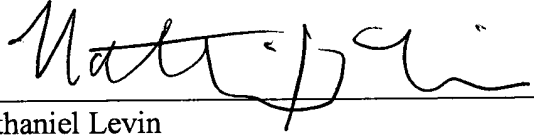
It is respectfully requested that FIG. 3 be amended by adding the PMOS transistors 340, 342 constituting the current mirror 338. It is not believed that this amendment introduces new matter inasmuch as the PMOS transistors 340, 342 are described in the specification at page 6, lines 17-20 of the specification as originally filed. The proposed amended FIG. 3 is attached hereto.

## R E M A R K S

Claims 25-38 are newly added. In addition, informalities in the specification and drawings (specifically, FIG. 3) are corrected. Applicant respectfully requests allowance of claims 1-38. If any issues remain, or if the Examiner has any further suggestions for expediting allowance of the present application, the Examiner is kindly invited to contact Nate Levin using the information provided below.

Respectfully submitted,

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